

Fig. 1 is a block diagram of a prior art system 5. The system 5 includes an array controller 25 connected to a plurality of storage devices 10, 15, 20, and 50. The storage devices 10, 15, 20, and 50 are arranged in a row and are connected to the array controller 25 via a common bus 7. The storage devices 10, 15, 20, and 50 are labeled A, B, C, and D, respectively.

5

Array
Controller

25

10

15

20

50

A

B

C

D

7

Prior Art

Fig. 1

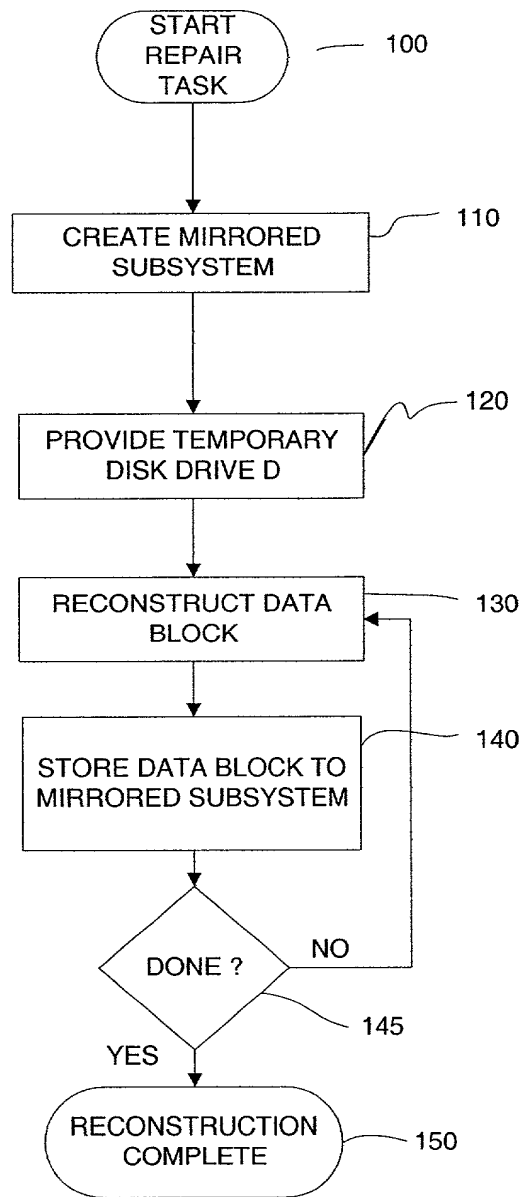


Fig. 2

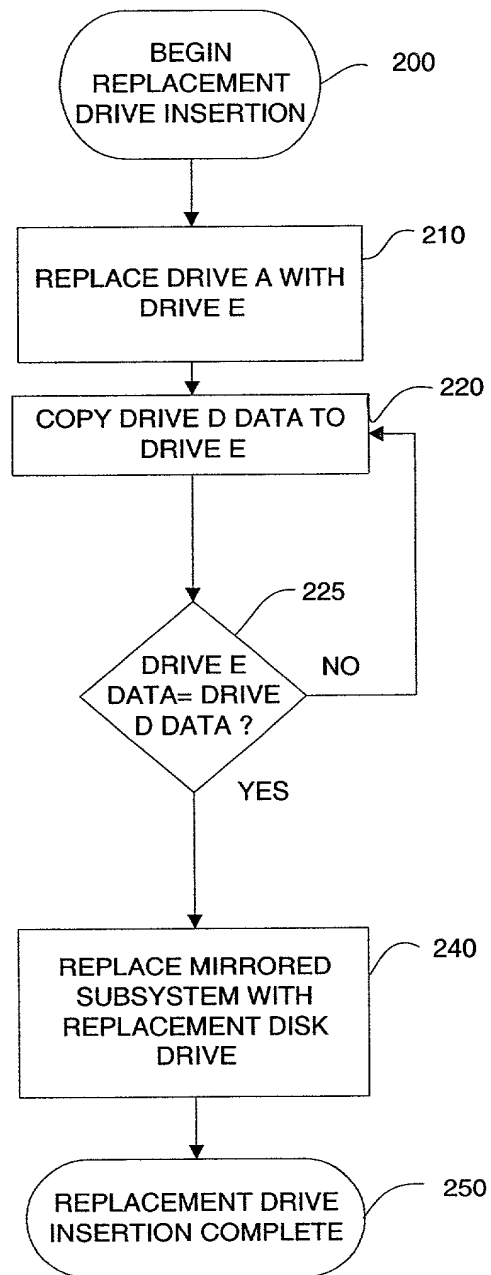


Fig. 3

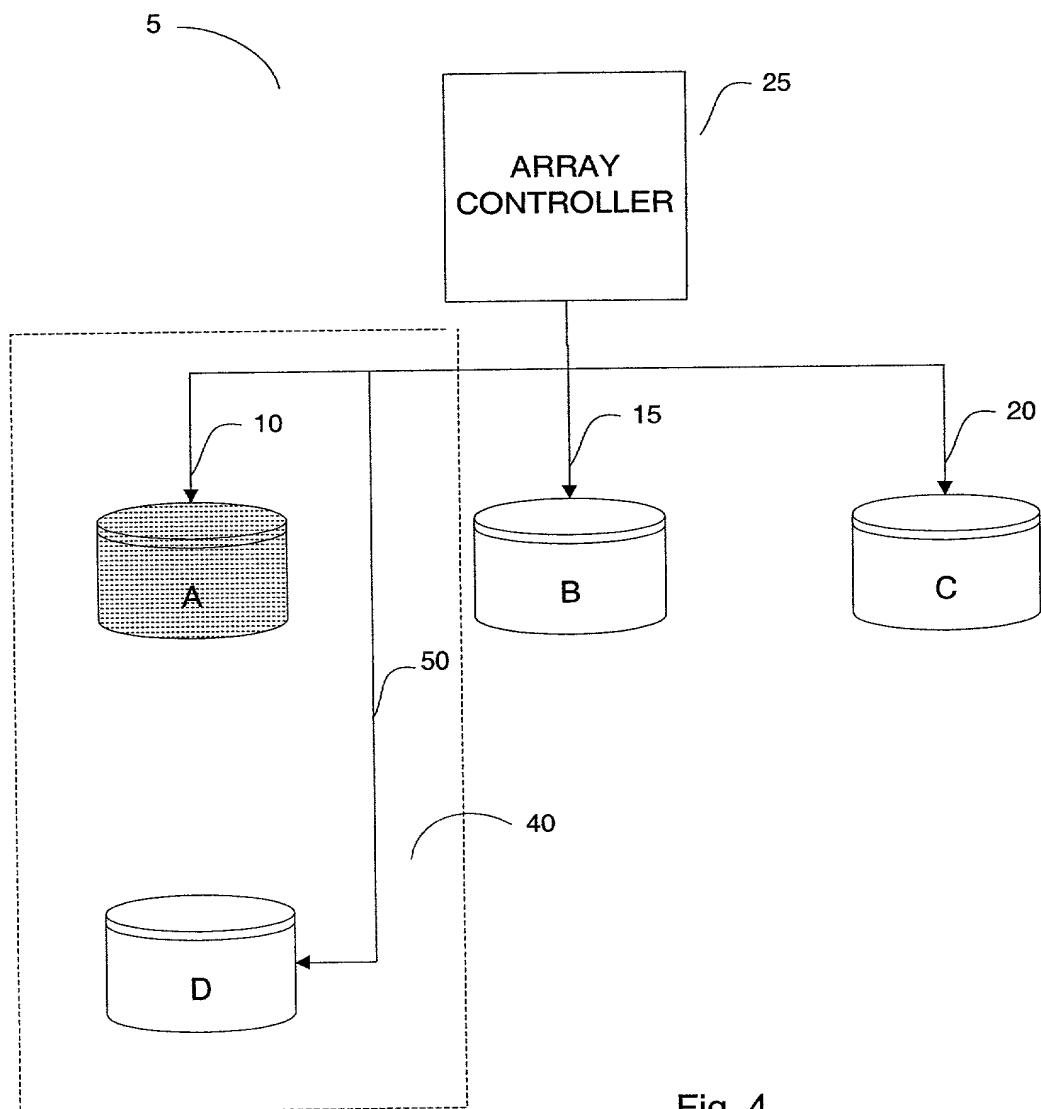


Fig. 4

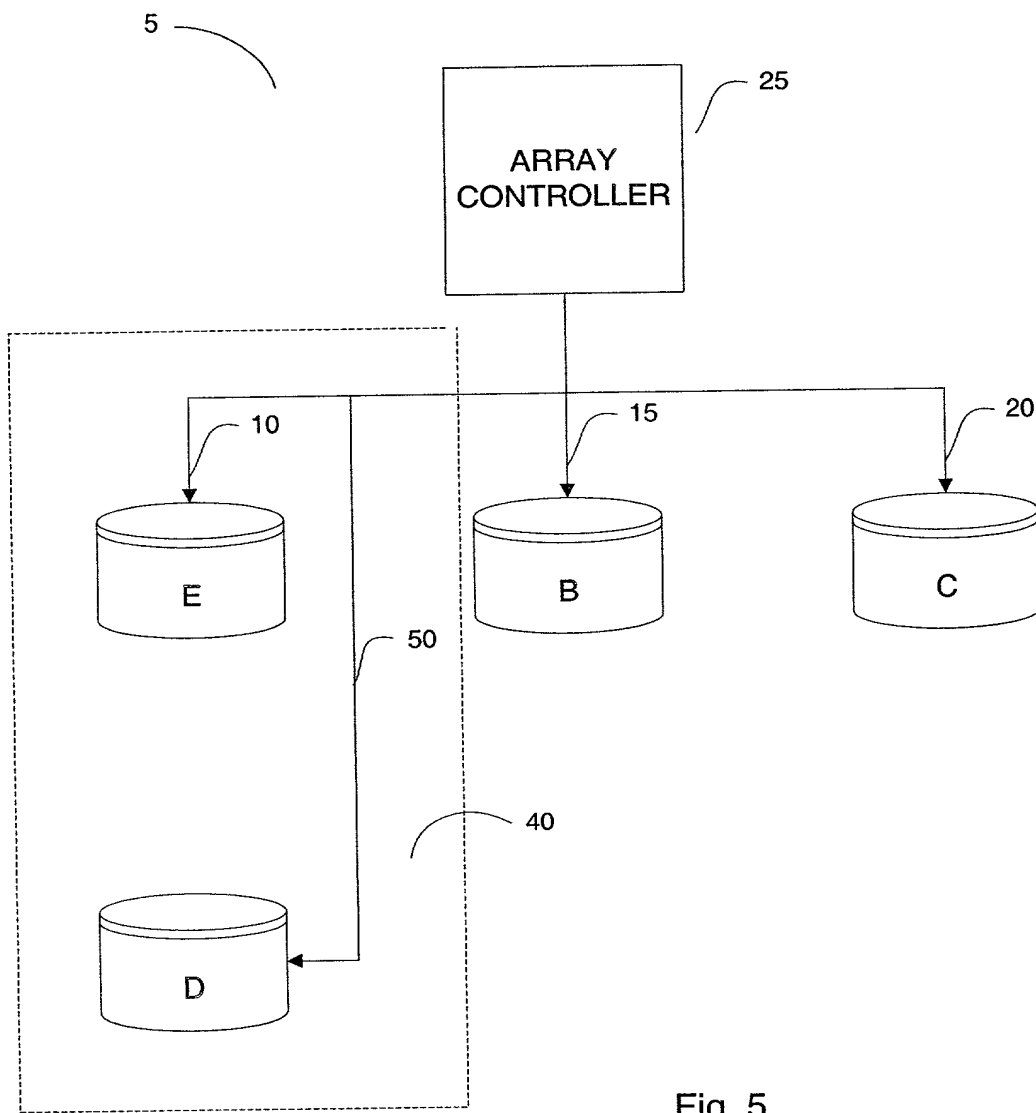


Fig. 5

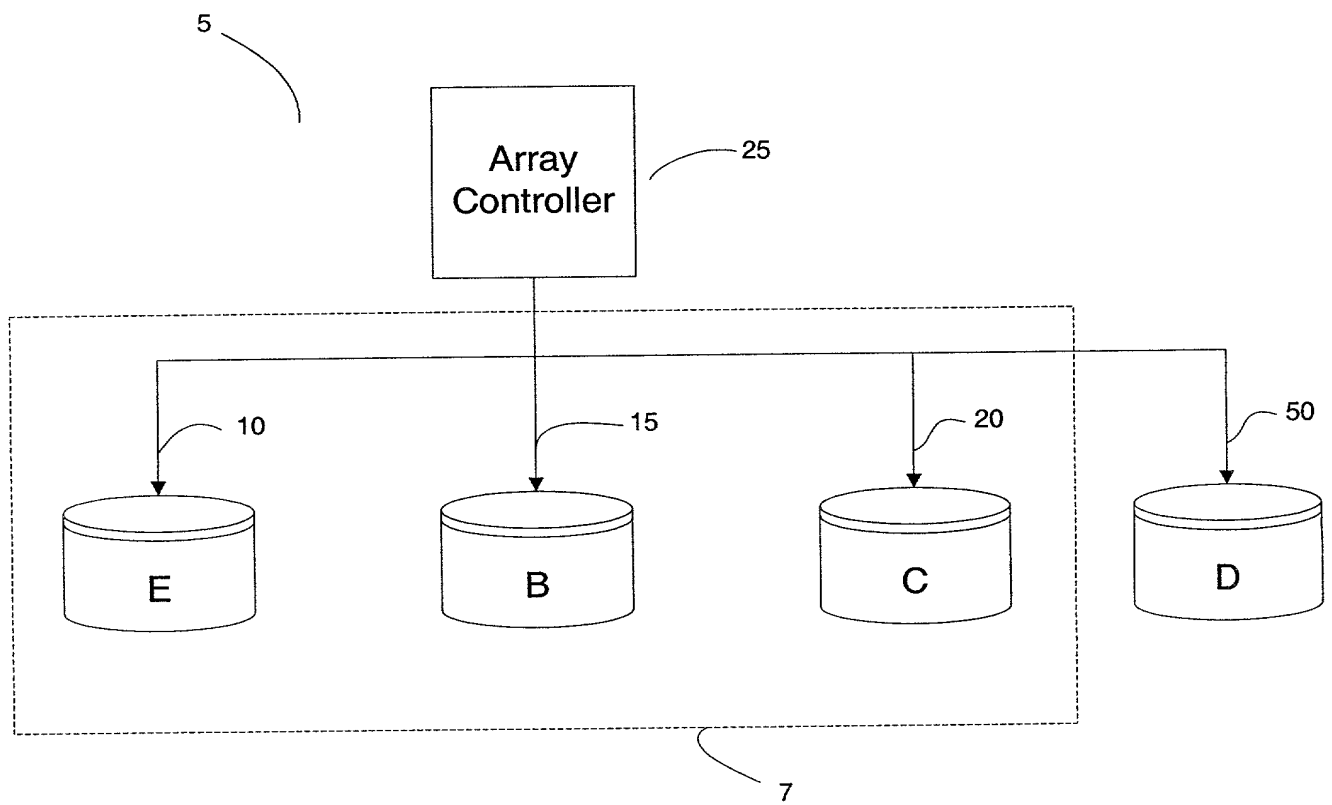
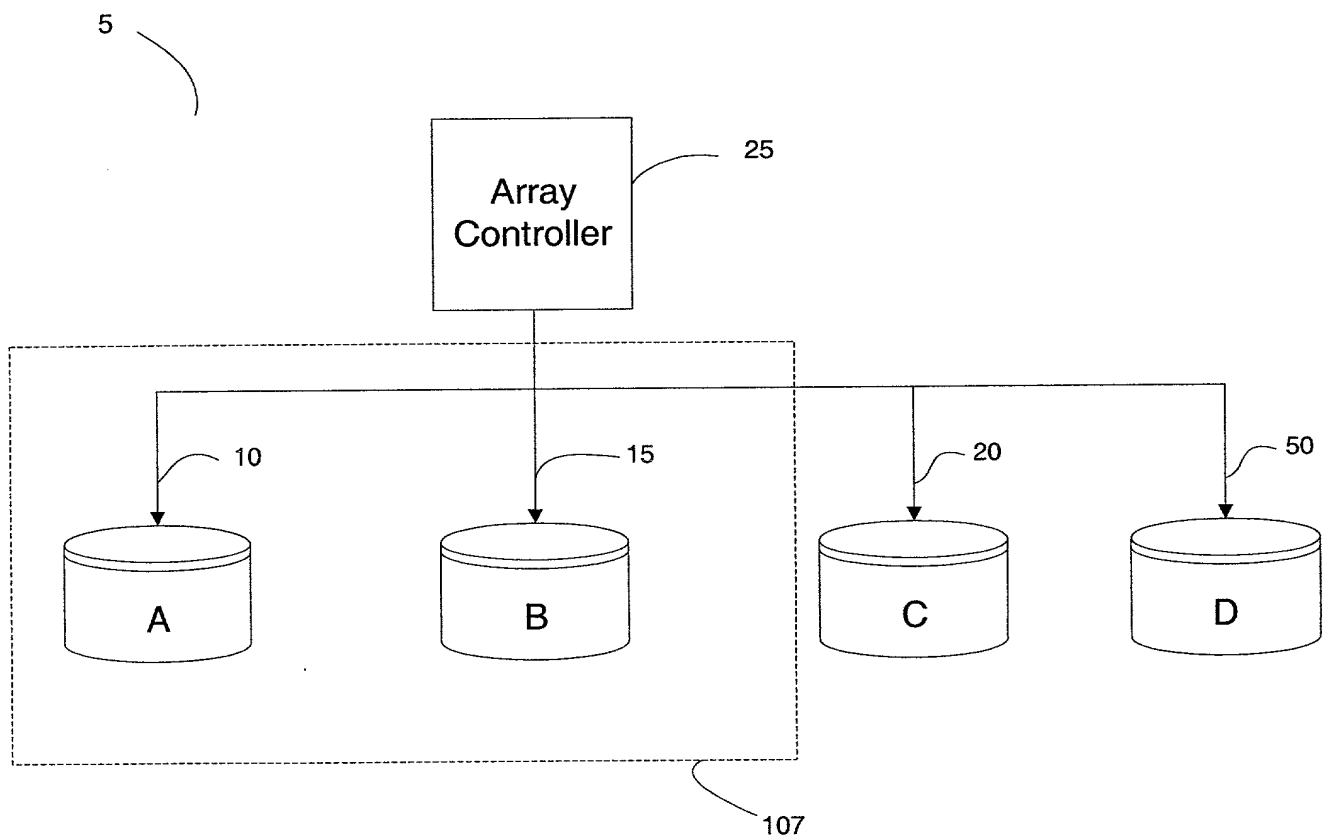


Fig. 6

Fig. 7



Prior Art

Fig. 7